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(54) **HIGH VOLTAGE LDMOS DEVICE WITH AN INCREASED VOLTAGE AT SOURCE (HIGH SIDE) AND A FABRICATING METHOD THEREOF**

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CPC H01L 29/7835; H01L 29/66659; H01L 29/1095; H01L 29/66681; H01L 29/7816
See application file for complete search history.

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(57) **ABSTRACT**

A high voltage LDMOS device having high side source voltage, an n type buried layer and a p type buried layer situated on the interface between a p type substrate and an n type epitaxial layer; a lateral surface of the n type buried layer and a lateral surface of the p type buried layer not in contact, and are distant from one another with a distance, thereby increasing the withstand voltage between the n type buried layer and the p type buried layer; the p type buried layer and the drain overlap at least partially in a vertical direction, enabling the p type buried layer to exert a reduced surface field action on the drain, to increase the withstand voltage of the drain against the source; the source and the body terminal centrally on top of the n type buried layer.

9 Claims, 4 Drawing Sheets